IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

ATTY.'S DOCKET: 00 P 9031 US

In re the application of: Helmut Tews et al.	)) Group Art: 2813
Serial No.: 09/714,356	) Examiner: Chen, Jack SJ.
Filing Date: November 16, 2000	)
Title: NITROGEN IMPLANTATION USING A SHADOW EFFECT TO CONTROL GATE OXIDE THICKNESS IN DRAM SEMICONDUCTORS	)

INFORMATION DISCLOSURE STATEMENT
UNDER 37 C.F.R. § 1.97 AND 1.98

Honorable Commissioner of Patents and Trademarks
Washington, D.C. 20231

Sir:

It is respectfully requested that the citations listed below be considered by the Patent and Trademark Office and made of official record in the above-identified application.

This Information Disclosure Statement is filed before the mailing date of any final action, a notice of allowance, or an action that otherwise closes prosecution in the application, and is accompanied by the fee set forth in §1.17(p) in the amount of $180.00.

In the opinion of the undersigned, the below-listed citations represents the closest art known to the undersigned during the preparation of the above-identified application. This citation may be material to the examination of the subject application and is therefore submitted in compliance with the duty of disclosure defined in 37 C.F.R. § 1.56 and 1.97.

A concise explanation of the relevance of the pertinent listed citations are set forth below.

CONCISE EXPLANATION OF THE RELEVANCE OF THE PERTINENT LISTED CITATIONS

U.S. Patent 5,330,920 is deemed pertinent for its disclosure of a method of controlling gate oxide thickness in the fabrication of semiconductor devices. The process comprises:

forming a sacrificial gate oxide layer on select locations of a semiconductor substrate surface;

implanting nitrogen ions into the select locations of the substrate through the sacrificial gate oxide layer;

thermally annealing the substrate and sacrificial gate oxide layer to assist pile-up of he nitrogen ions at the semiconductor substrate surface;

removing the sacrificial gate oxide layer; and

thermally forming a gate oxide layer on the silicon semiconductor substrate surface, wherein the select locations having nitrogen ion implanted will have a thinner gate oxide layer than a non-implanted region.

U.S. Patent No. 6,037,639 is deemed pertinent for its disclosure of fabrication of an integrated device using nitrogen implantation. The process comprises:

providing a channel region defined by a source and drain region of a semiconductor substrate having a gate structure comprising an isolating oxide layer positioned on the channel region and the polysilicon layer positioned on the oxide layer. More specifically, the process comprises forming the nitrogen implanted regions over the semiconductor substrate by implanting nitrogen atoms into those regions and growing spacers from exposed portions of the polysilicon layer. During the spacer growth, the spacer grows vertically as well as laterally extending under the polysilicon edges. Diffusion of nitrogen atoms to the substrate surface forms silicon nitride under the gate edges, which minimizes current leakages into the gate polysilicon.

U.S. Patent 5,920,779 is deemed pertinent for its disclosure of a process for differential gate oxide thickness by nitrogen implantation for mixed mode and embedded VLSI circuits comprising:

providing a semiconductor substrate having a surface, the semiconductor substrate comprising a first region on which a plurality of first MOS devices are to be formed and a second region on which a plurality of second MOS devices are to be formed;

masking the second region and providing a first concentration of a first dopant in the semiconductor substrate at the surface of the first region without doping the second region;

removing the mask over the second region;

masking the first region and providing a second concentration of a second dopant in the semiconductor substrate at the surface of the second region without doping the first region, wherein the second concentration is different than the first concentration;

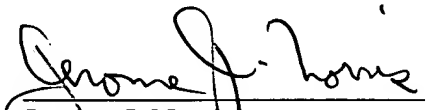
oxidizing the surface of the semiconductor substrate to grow a first thickness of oxide on the first region of the semiconductor substrate and to grow a second, different thickness of oxide on the second region in a single oxidizing process; and

forming first MOS devices on the first regions of the semiconductor substrate incorporating the first thickness of oxide and forming second MOS devices on the second region incorporating the second thickness of oxide;

wherein the first and second dopants are both nitrogen and the first concentration is greater than the second concentration.

This Disclosure Statement under 37 C.F.R. § 1.56 and 1.97 is not construed to the effect that no other material information as defined in 37 C.F.R. § 1.56(c) exist, or that this citation constitutes prior art under U.S.C. 102 and 103.

Respectfully submitted,



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